**PROJECT PROPOSAL**



**CSE-206L Electronic Circuits Lab**

**Group members:**

**NAME REG.NO**

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Class Section**: A**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Submitted to:

**Engr. Abdullah Hamid**

Data:(11,07,2021)

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

**Project name: -**

**“Digital adder with NPN BJT transistors”**

**Digital adder: -**

An adder is a [digital circuit](https://en.wikipedia.org/wiki/Digital_circuit) that performs [addition](https://en.wikipedia.org/wiki/Addition) of numbers. In many [computers](https://en.wikipedia.org/wiki/Computer) and other kinds of [processors](https://en.wikipedia.org/wiki/Microprocessor) adders are used in the [arithmetic logic units](https://en.wikipedia.org/wiki/Arithmetic_logic_unit) or ALU. They are also used in other parts of the processor, where they are used to calculate [addresses](https://en.wikipedia.org/wiki/Address_(computing)), table indices, [increment and decrement operators](https://en.wikipedia.org/wiki/Increment_and_decrement_operators) and similar operations.

Although adders can be constructed for many [number representations](https://en.wikipedia.org/wiki/Number_representation), such as [binary-coded decimal](https://en.wikipedia.org/wiki/Binary-coded_decimal) or [excess-3](https://en.wikipedia.org/wiki/Excess-3), the most common adders operate on [binary numbers](https://en.wikipedia.org/wiki/Binary_number). In cases where [two's complement](https://en.wikipedia.org/wiki/Two%27s_complement) or [ones' complement](https://en.wikipedia.org/wiki/Ones%27_complement) is being used to represent [negative numbers](https://en.wikipedia.org/wiki/Negative_number), it is trivial to modify an adder into an [adder–subtractor](https://en.wikipedia.org/wiki/Adder%E2%80%93subtractor). Other [signed number representations](https://en.wikipedia.org/wiki/Signed_number_representations) require more logic around the basic adder.

Basically the a half adder is simply an XOR gate (the cluster of 8 transistors in a diamond formation at the lower part of the circuit) to calculate the value of addition between two 1 bit binary numbers.

Classically a full adder is created with the use of 2 XOR gates, 2 AND gates and an OR gate. Each gate already consists of a fairfew transistors, especially the XOR gates, and thus the total number of transistors per classical full adder can reach 18.

A typical full adder is two half adders with an OR gate. The OR gate requires two transistors, which leaves us with 18 transistors per full adder (again, at least). This means that a 4-bit adder will require 62 transistors. Which also means that you'll need 124 transistors for your 8-bit adder.

**Project decision: -**

I Muhammad Ali and my project member Wajid Ullah are decided this project with mutual iinterest